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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/867,910	05/30/2001	Hisashi Adachi	MTS-3254US	7562

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/867,910	ADACHI ET AL.	
	Examiner	Art Unit	
	Juan A Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-10 and 15-22* is/are rejected.

7)☒ Claim(s) *4 and 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figures 15 and 16 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

The following lines should be deleted:

Page 10 lines 7, 11, 14, 17, 20 and 25.

Page 11 lines 3, 6, 9, 14, 17, 20 and 23.

Page 12 lines 5, 8 and 11.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains new subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification doesn't describe a **quadrature modulator** that includes two integrators of at least a second order integrating each of the converted digital I and Q signals using a second order integrator.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaji (US 5534827).

As per claim 1 Yamaji (US 5534827) discloses a transmitting circuit apparatus comprising: a first digital modulator (block 7) and a second digital modulator (block 8) for modulating an I signal and a Q signal which are multi-valued digital or analog baseband modulation signals, into a digital I signal and a digital Q signal, respectively, having the number of bits smaller than that of said baseband modulation signals; and a quadrature modulator for outputting a signal synthesized from the signals generated by

modulating (two) carrier waves each having a phase perpendicular to each other by using said modulated I and Q signals, respectively (figure 2 column 6 line 64 to column 7 line10).

As per claim 2 Yamaji (US 5534827) discloses a first and second digital modulators to modulate said I and Q signals which are multi-valued digital baseband modulation signals into two-valued digital I and Q signals, respectively (figure 2 column 6 lines 20-23).

As per claim 5. Yamaji (US 5534827) the use of a band-pass filter connected to the output of a quadrature modulator (figure 26 block 53 column 11 lines 63-65).

As per claim 6 Yamaji (US 5534827) discloses a quadrature modulator with a first and a second digital RF modulator each for performing amplitude modulation on each carrier waves having a phase perpendicular to each other, the modulated I and Q signals control the first and second digital RF modulators to perform amplitude modulation on said carrier waves, the modulated signals are synthesized into a signal, and the signal is then output (figure 2 column 6 line 64 to column 7 line10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji (US 5534827), and further in view of Karema (US 5061928). Yamaji (US 5534827) teaches claim 1 and 2. Yamaji (US 5534827) doesn't specify the order of the sigma-delta modulator. Karema (US 5061928) teaches the use of high-order sigma-delta modulators to increase the signal to noise ratio of the modulator. Sigma-delta modulator of order second and higher can be used in the modulator described by Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the quantification noise in the modulator described by Yamaji (US 5534827) to use a sigma-delta modulator of at least second order or higher.

As per claim 4 Yamaji (US 5534827) teaches claim 1 and 2. Yamaji (US 5534827) doesn't specify the use of a pass-band filter after the mixer in the I and Q modulator. It is very well know in the art and Yamaji (US 5534827) teaches the use of a band-pass filter for reducing unnecessary signals outside the transmission frequency band from the signals generated by modulating the carrier waves (figure 25 block 55 column 11 lines 58-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made when implementing the modulator described by Yamaji (US 5534827) to reduce unnecessary signals outside the transmission frequency band from the signals generated by modulating the carrier waves having a phase perpendicular to each other to include a band-pass filter after the mixer in the I and Q channels.

Claims 7, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji (US 5534827), and further in view of Camp (US 6194963)

As per claim 7 Yamaji (US 5534827) teaches claims 1,2 and 6. Yamaji (US 5534827) doesn't teach that each of said first and second digital RF modulators comprises a power amplifier, and each of the modulated I and Q signals controls the power supply of each power amplifiers to perform amplitude modulation on each of said carrier waves, and the amplitude-modulated signals are synthesized into an output signal of the quadrature modulator. Camp (US 6194963) teaches a power amplifier, where each of the modulated I and Q signals controls the power supply of each power amplifier to perform amplitude modulation (figure 1, column 2 lines 50-52). The power amplifier described by Camp (US 6194963) can be used in the modulator described by Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the efficiency of the power amplifiers, to include a method to control the power supply of the power amplifiers that perform amplitude modulation on each of said carrier waves, and the amplitude-modulated signals are synthesized into an output signal of the quadrature modulator as described by Camp (US 6194963).

As per claim 8 Yamaji (US 5534827) teaches claims 1,2 and 6. Yamaji (US 5534827) doesn't teach that the digital RF modulators comprises an amplitude modulator, a power amplifier and the carrier waves are modulated using the modulated I and Q signals by amplitude modulators, and then amplified by the power amplifiers the amplified signals are synthesized into an output signal of the quadrature modulator.

Camp (US 6194963) teaches a method to modulate independently the phase and the amplitude of the I and Q signals, modulating the amplitude using and amplitude modulator and a power amplifier. The method described by Camp (US 6194963) could be used in the modulator described by Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the number of components in the modulator to have independent phase and amplitude modulation in the I and Q signal using the amplitude modulator and the power amplifier described by Camp (US 6194963) when implementing the modulator of Yamaji (US 5534827).

As per claim 10 Yamaji (US 5534827) and Camp (US 6194963) teach claim 7. Camp (US 6194963) teaches that power amplifiers provide the RF output signal and constitutes a final amplifying stage, and hence no amplification circuit for the transmission signal is provided in the circuit in the stages after the quadrature modulator (column 1 lines 59-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the number of components in the modulator to have independent phase and amplitude modulation in the I and Q signal using the amplitude modulator and the power amplifier described by Camp (US 6194963) when implementing the modulator of Yamaji (US 5534827).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji (US 5534827), and further in view of Sugimura (US 6002301). Yamaji (US 5534827) teaches claim 6. Yamaji (US 5534827) doesn't teach the use of a dual-gate FET as a power amplifier. Sugimura (US 6002301) teaches that one conventionally well-known

power amplifier, especially a power amplifier for amplifying high-frequency signals, is the one which employs a dual-gate FET (column 1 lines 10-14). The modulator disclosed by Yamaji (US 5534827) could use the power amplifier disclosed by Sugimura (US 6002301). It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce power consumption, to use a power amplifier composed of a dual gate FET for the amplitude modulation with the modulated I and Q signals controls the output signal of the power amplifier via the second gate terminal of the dual gate FET to perform amplitude modulation on each carrier wave, and amplitude-modulated signals are synthesized into an output signal of the quadrature modulator in the system indicated by Yamaji (US 5534827) with the dual-gate FET described by Sugimura (US 6002301).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji (US 5534827), and further in view of Ribner (US 5682161). Yamaji (US 5534827) teaches claim 3. Yamaji (US 5534827) doesn't teach the use of a n-th-order integrator, a quantizer, and a feedback circuit, a value input to said n-th-order integrator undergoes n-th-order integration and is then input to said quantizer to be quantized into a digital value, the value serves as the output signal of said sigma-delta modulator, and at the same time, is in put to said feedback circuit, and the output signal of said feedback circuit is added to the input value of said sigma-delta modulator and the result is input to said n-th-order integrator. Ribner (US 5682161) teaches high-order sigma-delta modulators where the sigma-delta modulators comprises an n-th-order integrator, a quantizer, and a feedback circuit, a value input to said n-th-order integrator undergoes

n-th-order integration (figure 6 blocks 252, 254..), and is then input to a quantizer to be quantized into a digital value (figure 6 block 210), wherein said quantized value serves as the output signal of said sigma-delta modulator, and at the same time, is in put to said feedback circuit, and wherein the output signal of said feedback circuit is added to the input value of said sigma-delta modulator and the result is input to said n-th-order integrator (figure 6 column 6 lines 61-77 and equation 13). The modulator disclosed by Yamaji (US 5534827) could use the sigma-delta modulator disclosed by Sugimura (US 6002301). It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve the precision of the sigma-delta modulator to implementing the system indicated by Yamaji (US 5534827) with a n-th order delta-sigma modulator use the modulator described by Ribner (US 5682161).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji (US 5534827), and further in view of Ritoniemi (US 5629701). Yamaji (US 5534827) teaches claim 3. Yamaji (US 5534827) doesn't teach that the sigma-delta modulator comprises a plurality of lower-order sigma-delta modulators connected in multi-stage, the output signal of each of said plurality of lower-order sigma-delta modulators is synthesized by connecting the output to a differentiator having a configuration expressed by a z transform $(1-z^{-1})^{m}$ with the degree m up to the preceding stage. Ritoniemi (US 5629701) teaches a plurality of lower-order sigma-delta modulators connected in multi-stage, the output signal of each of said plurality of lower-order sigma-delta modulators is synthesized by connecting the output to a differentiator having a configuration expressed by a z transform $(1-z^{-1})^{m}$ with the degree m up to the preceding

stage (figure 1 column 3 lines 51-66). The modulator disclosed by Yamaji (US 5534827) could use the sigma-delta modulator disclosed by Ritoniemi (US 5629701). It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the quantizing error of the sigma-delta modulator in the system indicated by Yamaji (US 5534827) to use a plurality of lower order sigma-delta modulators with a differentiator in the way described by Ritoniemi (US 5629701).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji (US 5534827), and further in view of Borth (US 4775851). Yamaji (US 5534827) teaches claim 3. Yamaji (US 5534827) doesn't teach that the output the sigma-delta modulators is provided with a digital filter having low-pass characteristics. Borth (US 4775851) teaches a sigma-delta modulator where the output of the sigma-delta modulators is provided with a digital filter having low-pass characteristics (figure 3, column 8 lines 7-10). The modulator disclosed by Yamaji (US 5534827) could use the sigma-delta modulator follow with the low-pass FIR filter disclosed by Borth (US 4775851). It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the out of band quantification noise of the sigma-delta modulator in the system indicated by Yamaji (US 5534827) to use a low-pass FIR filter at the output of the sigma-delta modulator the way described by Borth (US 4775851).

Claims 18, 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cojocaru (US 6339621), and further in view of Yamaji (US 5534827).

As per claim 18 Cojocaru (US 6339621) discloses a method comprising the steps of:(a) receiving baseband I and Q multi-valued digital signals, each signal represented

by n-bits (figure 4 input of blocks 102 and 104, column 5 lines 3-5); (b) converting each of the signals received in step (a) into digital I and Q signals, respectively, represented by less than n-bits (figure 4 blocks 106 and 108, column 5 lines 39-41); (c) modulating the converted digital I and Q signals of step (b) using a quadrature modulator (figure 4 blocks 112 and 114, column 5 lines 42-45). Cojocaru (US 6339621) doesn't teach transmitting the modulated signals of step (c). Yamaji (US 5534827) teaches transmitting the modulated signals of step (c) (figure 27, column 12 lines 5-7). The modulator disclosed by Cojocaru (US 6339621) could use the transmitter disclosed by Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to send the modulated signal described by Cojocaru (US 6339621) to use a transmitter in the way described by Yamaji (US 5534827).

As per claim 19 Cojocaru (US 6339621) discloses a method comprising the steps of:(a) receiving baseband I and Q multi-valued digital signals, each signal represented by n-bits (figure 4 input of blocks 102 and 104, column 5 lines 3-5); (b) converting each of the signals received in step (a) into digital I and Q signals, respectively, represented by less than n-bits (figure 4 blocks 106 and 108, column 5 lines 39-41) representing each of the digital I and Q signals by two-bits (column 2 lines 21-22); (c) modulating the converted digital I and Q signals of step (b) using a quadrature modulator (figure 4 blocks 112 and 114, column 5 lines 42-45). Cojocaru (US 6339621) doesn't teach transmitting the modulated signals of step (c). Yamaji (US 5534827) teaches transmitting the modulated signals of step (c) (figure 27, column 12 lines 5-7). The modulator disclosed by Cojocaru (US 6339621) could use the transmitter disclosed by

Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to send the modulated signal described by Cojocaru (US 6339621) to use a transmitter in the way described by Yamaji (US 5534827).

As per claim 20 Cojocaru (US 6339621) discloses a method comprising the steps of:(a) receiving baseband I and Q multi-valued digital signals, each signal represented by n-bits (figure 4 input of blocks 102 and 104, column 5 lines 3-5); (b) converting each of the signals received in step (a) into digital I and Q signals, respectively, represented by less than n-bits using a sigma-delta modulator (figure 4 blocks 106 and 108, column 5 lines 39-41); (c) modulating the converted digital I and Q signals of step (b) using a quadrature modulator (figure 4 blocks 112 and 114, column 5 lines 42-45). Cojocaru (US 6339621) doesn't teach transmitting the modulated signals of step (c). Yamaji (US 5534827) teaches transmitting the modulated signals of step (c) (figure 27, column 12 lines 5-7). The modulator disclosed by Cojocaru (US 6339621) could use the transmitter disclosed by Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to send the modulated signal described by Cojocaru (US 6339621) to use a transmitter in the way described by Yamaji (US 5534827).

As per claim 21 Cojocaru (US 6339621) discloses a method comprising the steps of:(a) receiving baseband I and Q multi-valued digital signals, each signal represented by n-bits (figure 4 input of blocks 102 and 104, column 5 lines 3-5); (b) converting each of the signals received in step (a) into digital I and Q signals, respectively, represented by less than n-bits (figure 4 blocks 106 and 108, column 5 lines 39-41); (c) modulating

the converted digital I and Q signals of step (b) using a quadrature modulator (figure 4 blocks 112 and 114, column 5 lines 42-45). Cojocaru (US 6339621) doesn't teach (c1) amplifying each of the converted digital I and Q signals, and synthesizing the amplified I and Q signals prior to the transmitting step and (d) transmitting the modulated signals of step (c). Yamaji (US 5534827) teaches amplifying each of the converted digital I and Q signals (column 11 line 60) as in claim 8, and synthesizing the amplified I and Q signals prior to the transmitting step (figure 2 block 6 column 7 lines 7-9) and (d) transmitting the modulated signals of step (c) (figure 27, column 12 lines 5-7). The modulator disclosed by Cojocaru (US 6339621) could use the transmitter disclosed by Yamaji (US 5534827). It would have been obvious to one of ordinary skill in the art at the time the invention was made to send the modulated signal described by Cojocaru (US 6339621) to use a transmitter in the way described by Yamaji (US 5534827).

Allowable Subject Matter

Claims 4 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A Torres whose telephone number is (571) 222-3119. The examiner can normally be reached on Tuesday-Thursday 9:00- 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H Ghayour can be reached on (571) 222-3021. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT 10/1/2004

JAT

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